



SFU CSDL



“Design Considerations for InAs/AISb HFETs”

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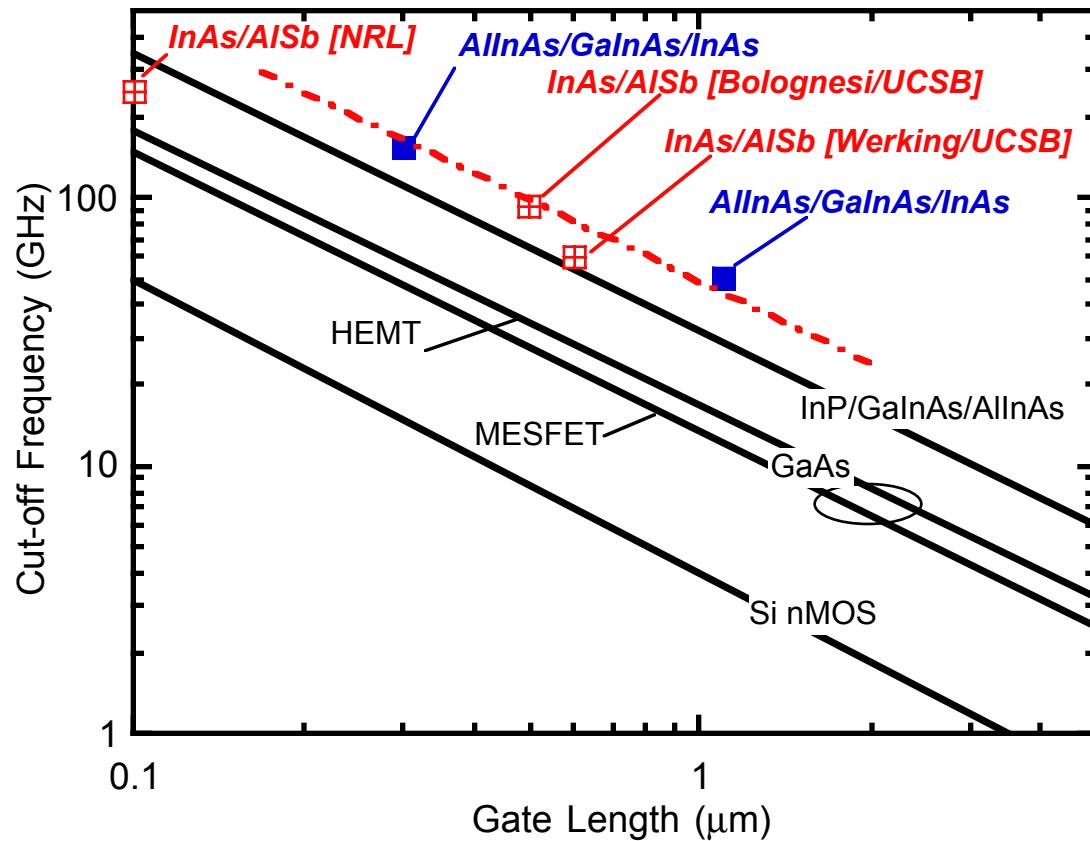


Outline

- *Potential Performance of InAs HFETs*
- *Band Lineups: Assets and Liabilities*
- *Ionization Hole Charge*
- *Quantum Confinement Effects*
- *Bandgap Engineered Solution*
- *A Proposed “Ultimate InAs HFET”*
- *Other SFU Good Stuff for Low Voltage Applications*



Potential Performance: THz Bandwidth?



- **InAs Channel HFETs can Exceed 1 THz BW for the Deep Submicron**
- **Not Clear which of InAs/AISb or InAs/AllnAs/InP is the Best Choice**
- **InP-Based has the Advantage of Maturity**



Band Lineups: Assets & Liabilities

Pros:

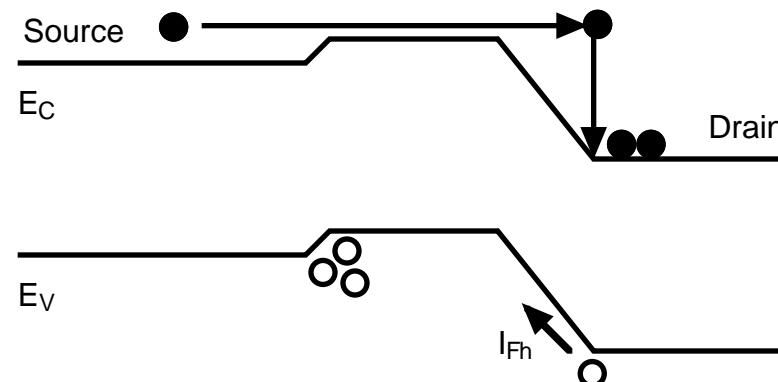
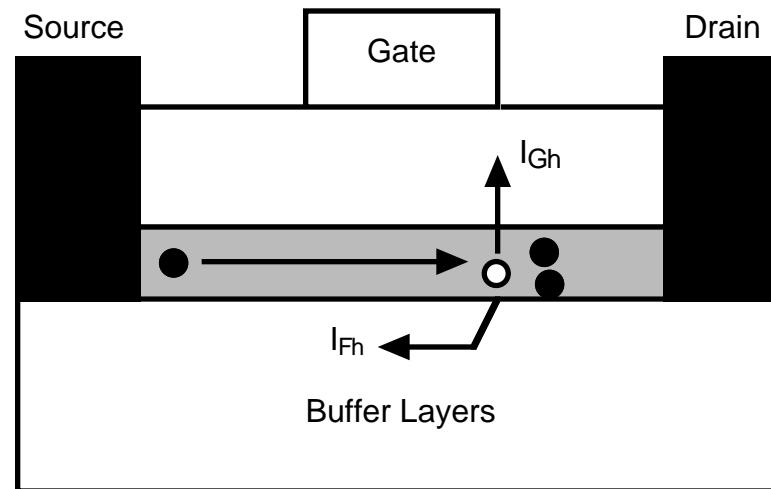
- *Deepest QWs — High Modulation Efficiency*
- *High Electron Mobilities, Peak Velocities*

Cons:

- *Type II Lineup*
 - *No Hole Confinement*
 - *Gate Leakage Current due to Impact Ionization*
 - *Low Breakdown Voltages*
 - *Very Complex RF Small Signal Behavior*
 - *Prone to Kink Effect*

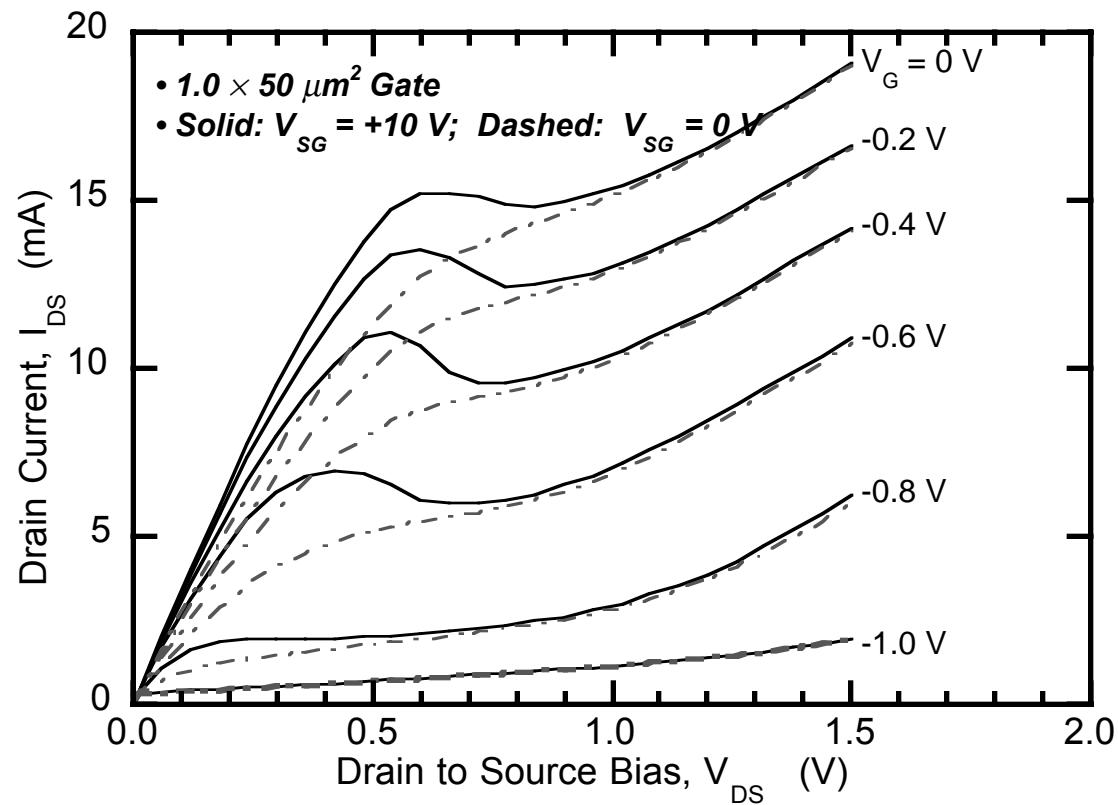


Impact Ionization Hole Charge





Effects of Parasitic Hole Charge: Sidegating



- Major Distortions in I-V Curves
- Injected by Ionization (Kink), sidegate, etc.

Bolognesi, Dvorak & Chow Jpn. J. Appl. Phys. 36 p. 1789 (1997)

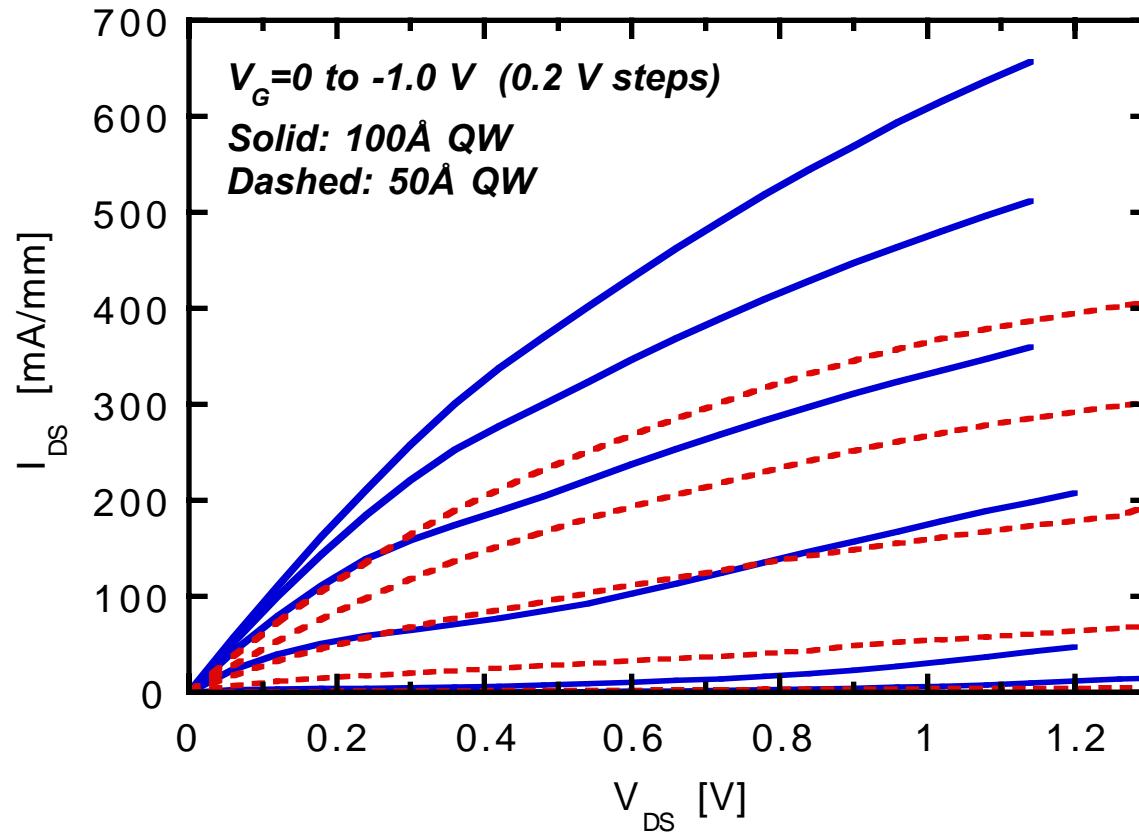


Quantum Confinement Effects

- ***Deep QWs, Quantization > $E_{G,InAs}$ Possible!***
- ***Increase Ionization Threshold***
- ***Reduce Parasitic Ionization Hole Charge***
- ***Increase Breakdown Voltage***
- ***Decrease Gate Leakage Currents***
- ***Increase F_{MAX} , Reduce G_{DS}***
- ***Compared Performance of 50 and 100Å Channels***



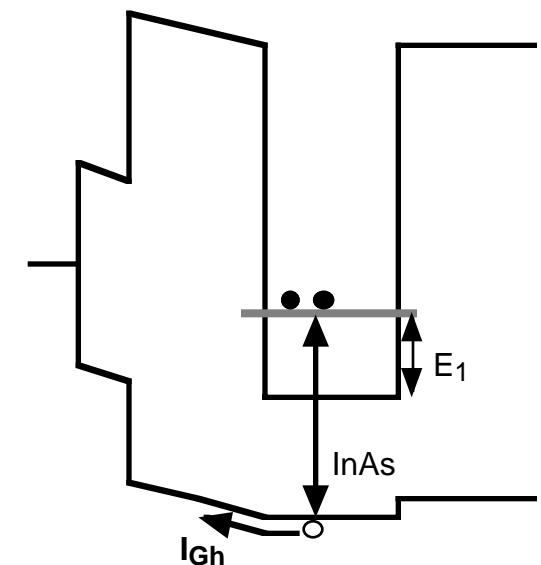
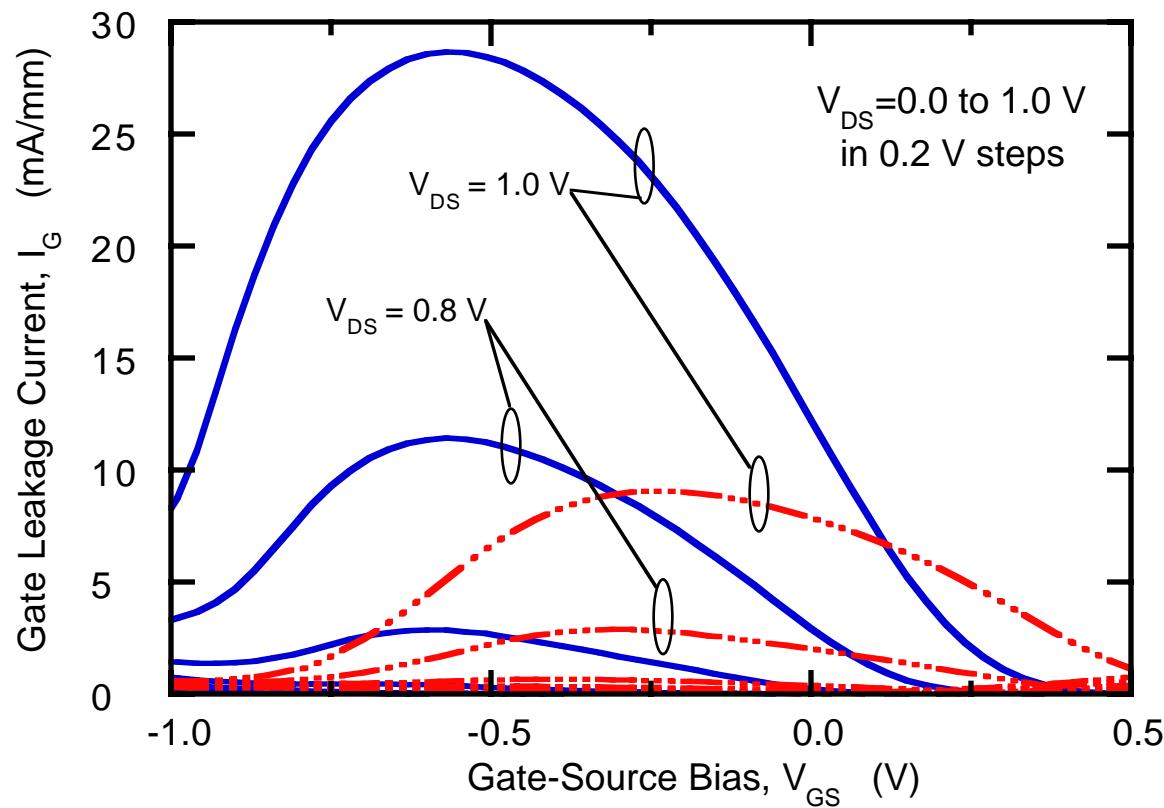
I-V Curves ($0.6\mu m$ Gates)



- Reduced Kink and G_{DS}
- Reduced G_M and Current Drive Due to Lower Mobility
- Interface Roughness Scattering Reduces Mobility



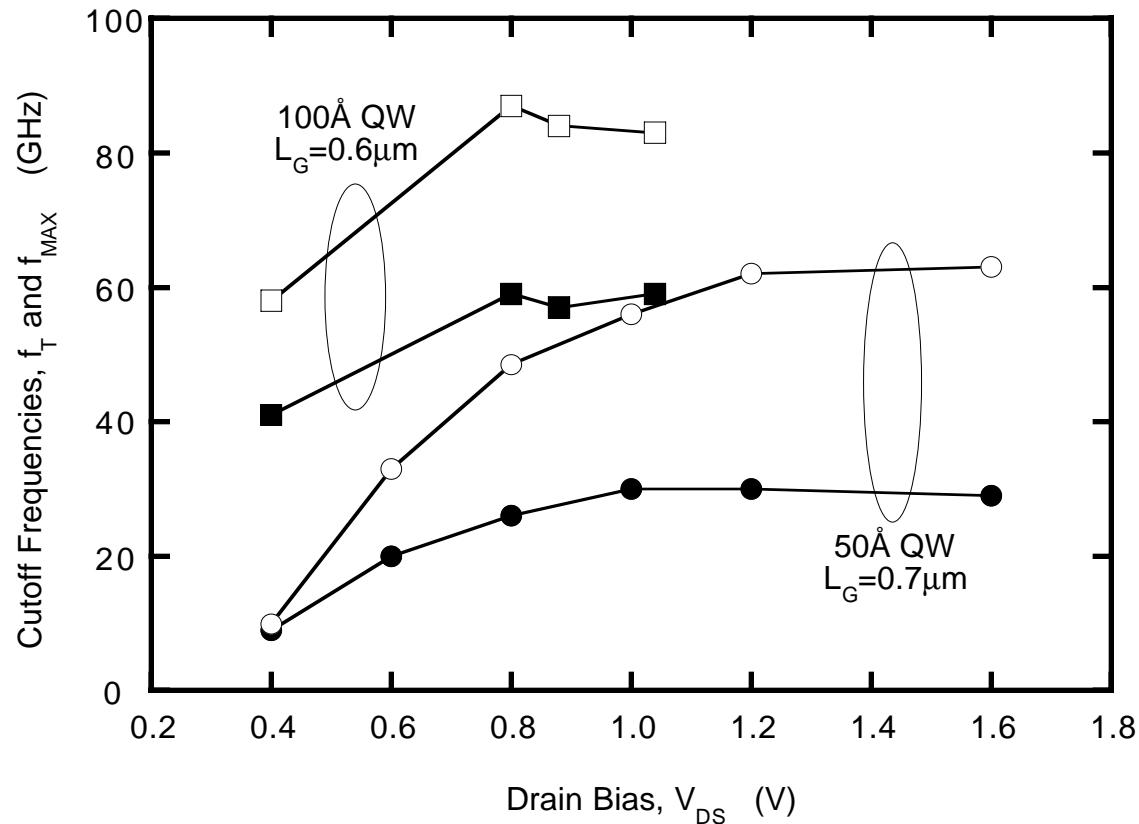
Gate Leakage: Impact Ionization Monitor



- 4X Reduction of Ionization Rate by a ~0.2eV Increase in Gap
- Ionization Effects Delayed by $\Delta V_{DS} = 0.2$ V
- Demonstration of In-Plane Increase in Ionization Threshold by QC



RF Effects of Quantum Confinement



- F_{MAX}/F_T Ratio Increased in Narrower QW
- F_T is Reduced due to Interface Roughness Scattering (IFRS)

C. R. Bolognesi et al., APL 61 (2) p. 213 (1992).



Effect of Well Width on Average Velocity (Measurements as a function of gate length)

$$\frac{1}{2\pi f_T} = \frac{L_G}{v_{\text{eff}}} + \frac{\Delta L}{v_{\text{eff}}} = \tau_T$$

QW	$\mu_{300K} \text{ (cm}^2/\text{Vs)}$	$v_{\text{eff}} (\times 10^7 \text{ cm/s})$
50 \AA	$9,000$	~ 2.5
100 \AA	$21,000$	~ 4.0

Low-Field Mobility Does Matter!!!

(Even if some would have us believe that only saturated velocity counts...)

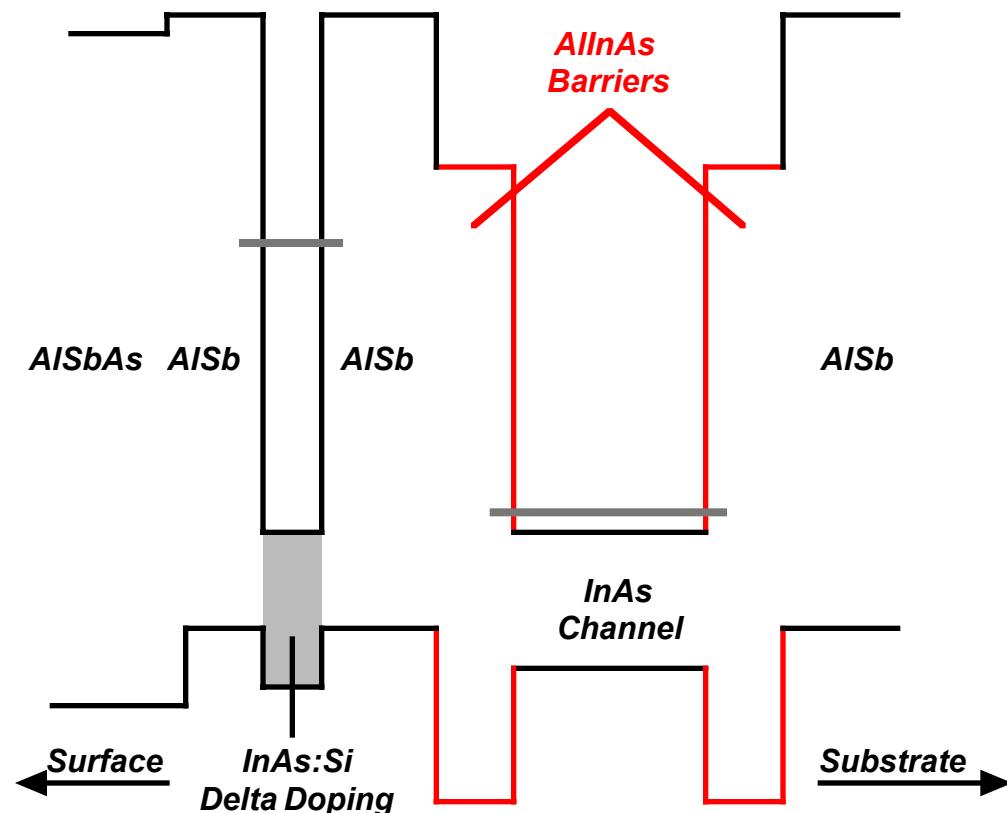


Quantum Confinement: Conclusions

- ***Quantization is Effective, but...***
- ***Not a Viable Approach unless InAs/AISb Interface Quality can be Improved (IFRS Reduction of Mobility and Average Channel Velocity)***
- ***IFRS Setbacks InAs/AISb to Performance Levels Achievable in InAlAs/GaInAs/InP HEMTs!***
- ***Bandgap Engineered Alternative Needed***
 - ***Must Maintain Mobility (to beat InP HEMTs)***
 - ***Must Prevent Holes From Reaching Buffer***



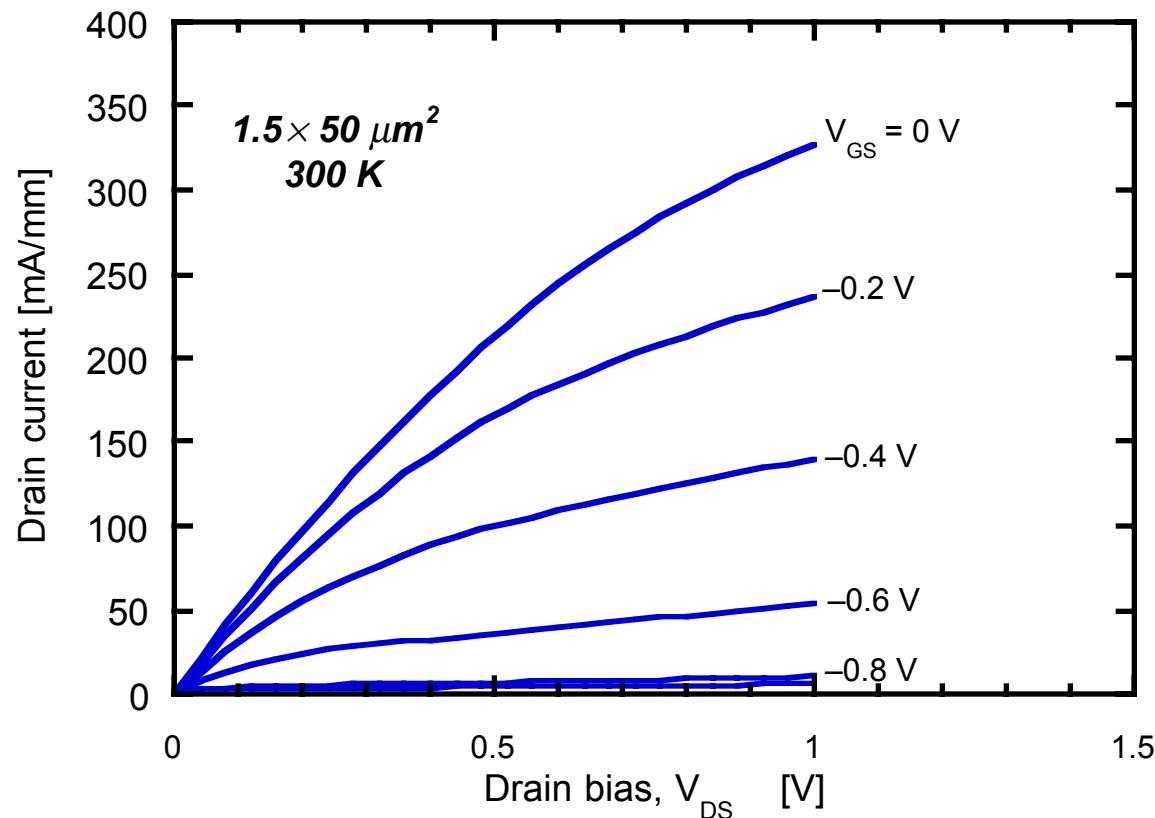
“Bandgap-Engineered” Channels ©



- **Form “Type I” Channel with Strained AllnAs Barriers**
- **Confine Impact Ionization Holes & Prevent Accumulation in Buffer**



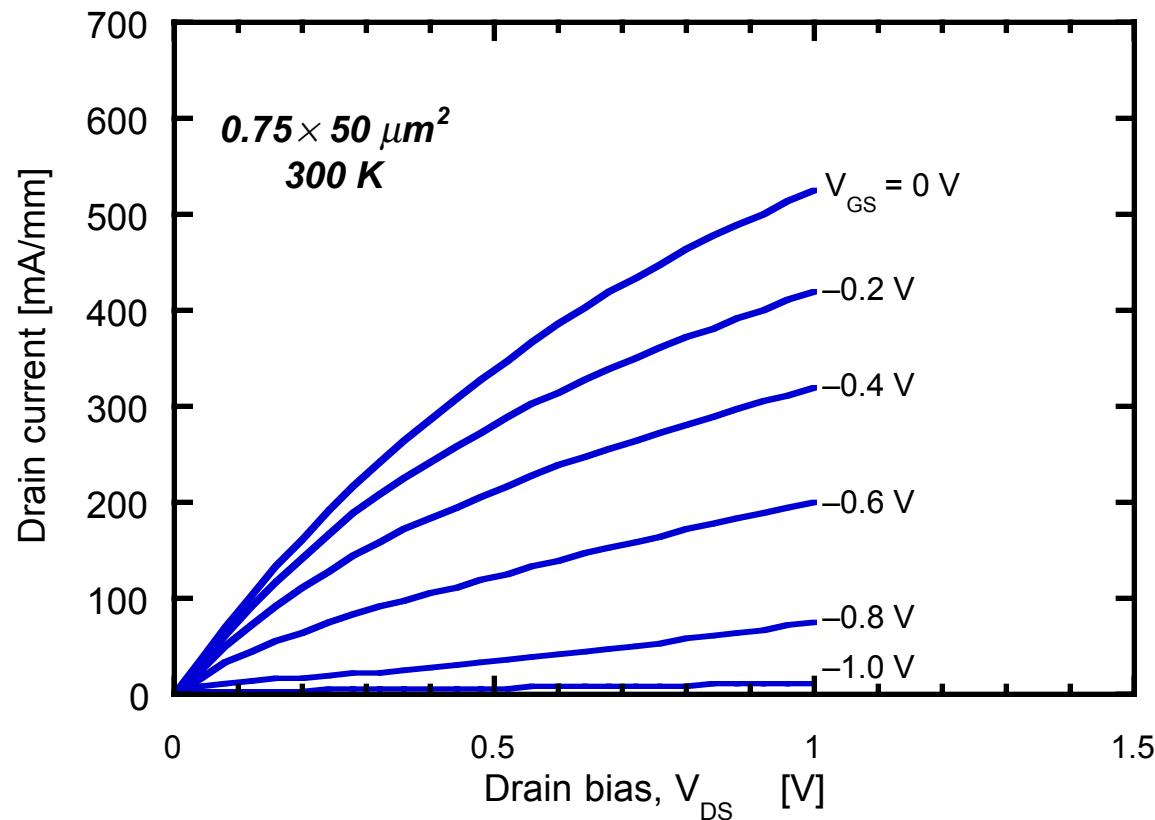
Kink-Free $1.5\mu\text{m}$ InAs/AlSb HFETs



- *Kink-Free Devices (2nd Derivative Negative Except Near Pinch-Off)*
- *What About Submicron Behavior?*



Well-Behaved $0.75\mu\text{m}$ InAs/AISb HFETs



- Very Nearly Kink-Free Devices
- $F_T = 40 \text{ GHz}$ $F_{MAX} = 65 \text{ GHz}$ for $0.75 \mu\text{m}$
- $\mu = 16,000 \text{ cm}^2/\text{Vs}$ $N_S = 1.1 \times 10^{12} \text{ cm}^{-2}$ ($Sb1752 / 20\text{\AA} Al_{0.3}In_{0.7}As$)



AISb/AInAs/InAs HFETs: Summary

- *Proof of Concept, Preliminary Result*
- *Growth Requires Optimization*
 - *Mobility*
 - *Sheet Density*
- *Band Structure Approach*
 - *More Effective than Doping Schemes*
- *Improved RF Behavior*
 - See *IPRM'98 re: RF Non-Idealities*



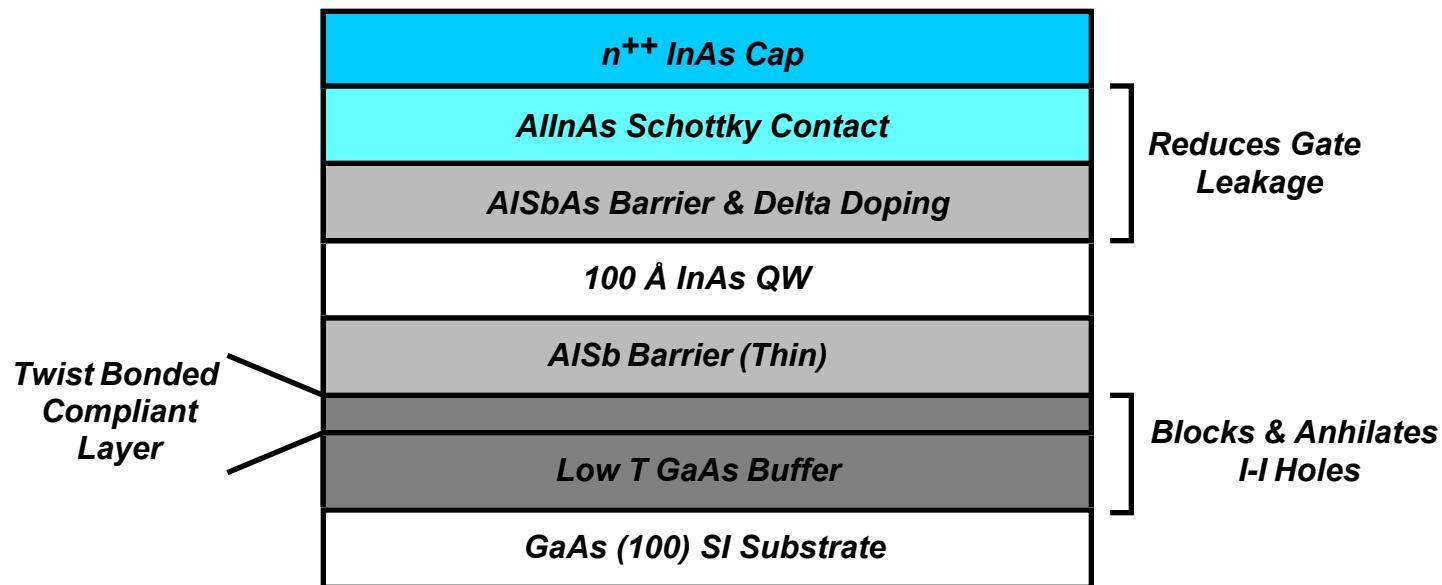
AISb/InAs HFETs: What's Next?

- Remove Ionization Hole Charge
 - Rather than Suppressing Ionization
- Reduce Growth Time
 - 3 μm Buffers are not Competitive ($t = \$$)
- What about the Role of Dislocations?
- Reduce Gate Leakage
 - AllInAs Top Barrier, as per NRL

If the above can be done, we might have the ultimate HFET!



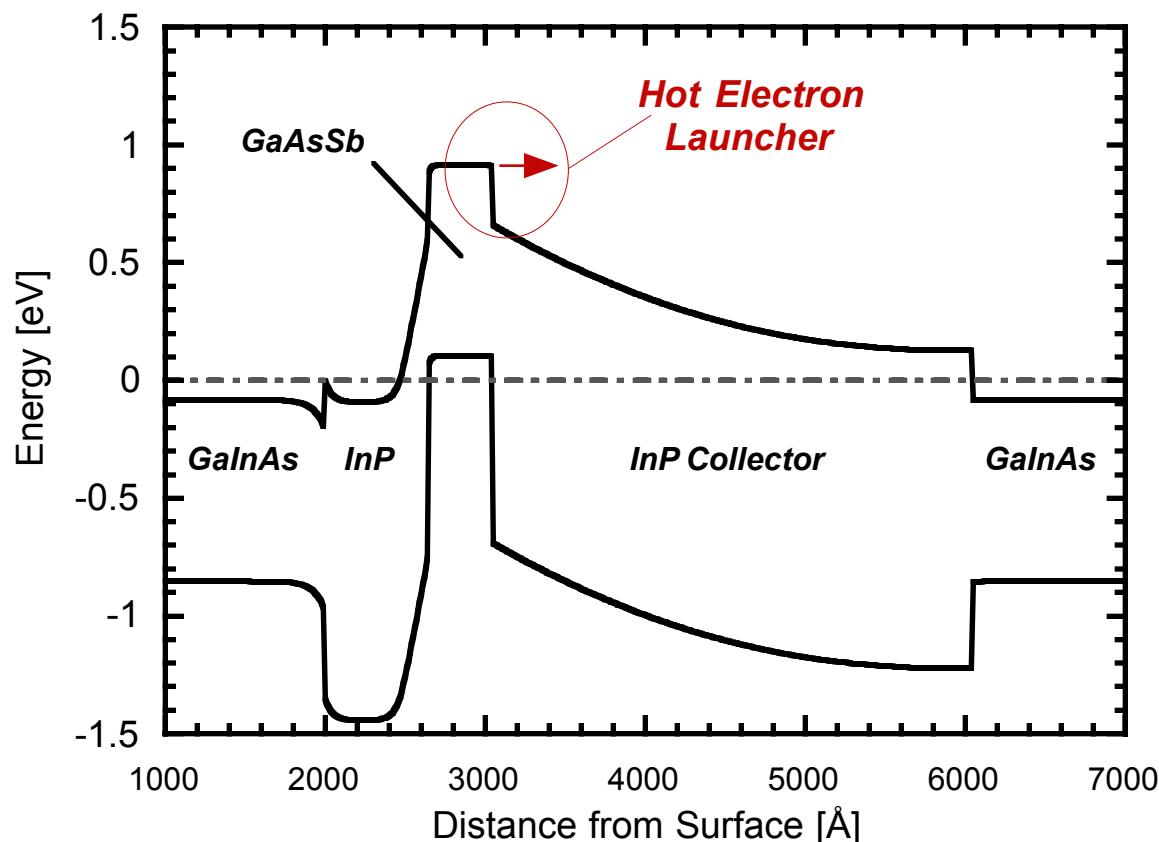
The “Ultimate” InAs/AISb HFET ©



- ***Dislocation-Free***
- ***Kink-Free***
- ***Ultra-High F_T with Good F_{MAX}***
- ***Expensive to Make***
- ***Is it Worth the Effort?***



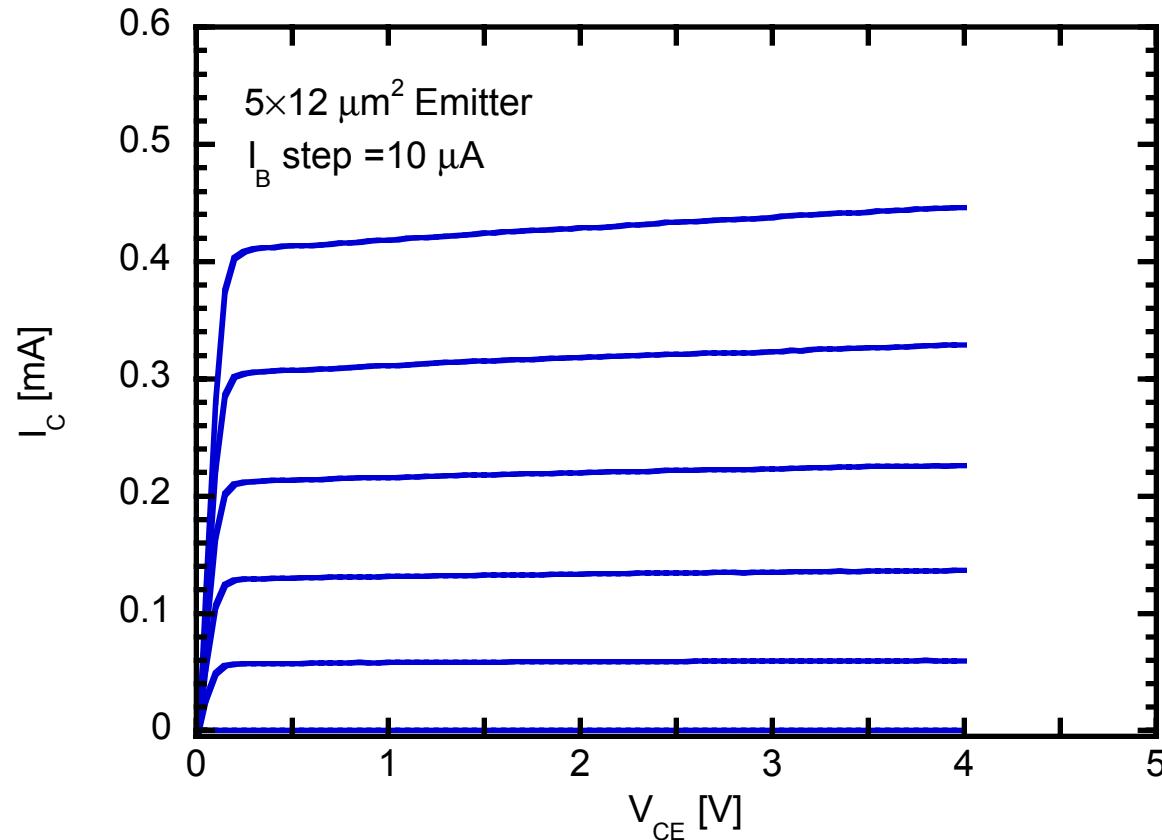
Other Antimonide-Enabled Concept: InP/GaAsSb/InP DHBTs





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$5 \times 12 \mu\text{m}^2$ DHBT: $V_{CE,\text{off}} = 12 \text{ mV}$

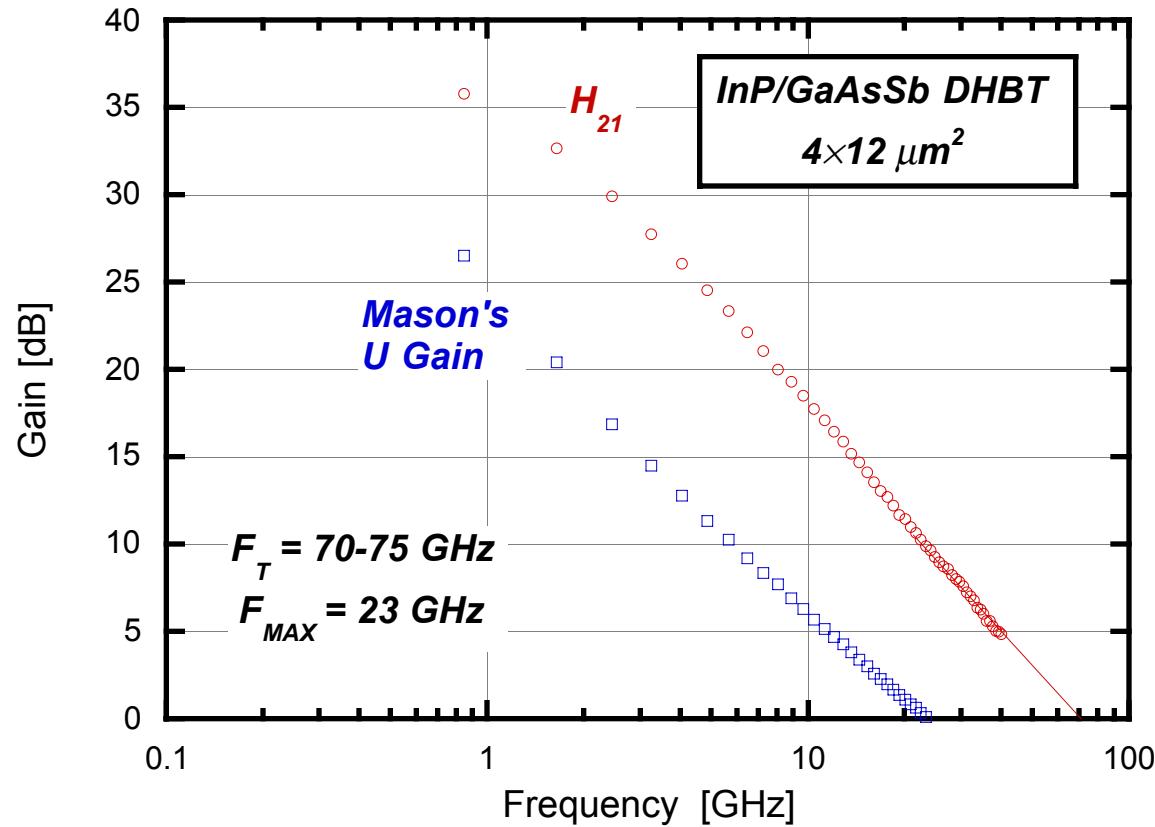


$$V_{CE,\text{off}} = R_E I_B + \frac{n k T}{q} \ln \frac{A_C}{A_E} + \frac{n k T}{q} \ln \frac{J_{SC}}{J_{SE}}$$



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Preliminary F_T and F_{MAX} (GaAsSb)



- Limited by $R_{BB}C_{CB}$
- Collector Doping & Base R_{SH} ($1400 \Omega/\square$)



GaAsSb HBT Summary (see 1998 DRC)

- **Very Low Offset Voltages (ΔV_{CE})**
- **Very Low E/B Turn-On Voltages**
- **Attractive for Low-V Wireless**
- **No Current Blocking at Collector**
- **Grading-Free Heterojunctions**
- **Ideal Gummel Characteristics (Forward & Reverse)**
- **Not Sensitive to Surface Recomb. (P/A)**
- **Demonstration of High-Gain RF Devices**
- **RF Performance Limited by Collector Doping Tail**
- **Fully Thermal Base Injection**

Prediction: 200 GHz F_T & F_{MAX} with $BV_{CEO} \geq 7V$